PATENT ABSTRACTS OF JAPAN

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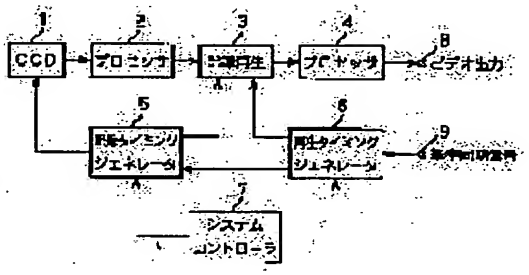
(72)Inventor : TONOMURA MASAHARU

(54) VIDEO CAMERA AND ITS CONTROL METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To simply and easily realize time base conversion without changing a filter characteristic and a delay amount or the like and without making a timing synchronization circuit of the recording system and the reproduction system complicated.
SOLUTION: An image signal photographed by a CCD imager 1 is recorded/ reproduced by a recording and reproducing section 3 and time expansion or compression of the video image is conducted in this video camera. The camera is provided with a recording timing generator 5 that generates a drive signal for the CCD imager 1 and a recording timing signal. The recording timing generator 5 processes a timing at reading of the image signal from the CCD imager 1 and at recording of the image signal as a packet in the unit of fields so as to make a data rate in the packet constant to be an unmagnified rate.



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[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

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CLAIMS

[Claim(s)]
[Claim 1] While performing record playback of a picture signal picturized with an image sensor, it is the video camera which can perform time-axis elongation or compression of an image. It has a timing generating means to generate a driving signal of the above-mentioned image sensor, and a timing signal at the time of record at least. The timing generating means concerned a video camera characterized by making a data rate in the packet concerned fixed-ize while a picture signal from the above-mentioned image sensor carries out reading appearance and treating timing at the time of record of the picture signal concerned as a packet of 1 field unit.
[Claim 2] The above-mentioned timing generating means is a video camera according to claim 1 characterized by making between from a sensor gate pulse to the above-mentioned image sensor to the Rhine shift termination of the 1 field into the above-mentioned packet.
[Claim 3] The above-mentioned timing generating means is a video camera according to claim 1 characterized by making 1X fixed-ize a data rate in the above-mentioned packet.
[Claim 4] The above-mentioned timing generating means is a video camera according to claim 1 characterized by also generating a timing signal at the time of playback of a recorded picture signal, and generating timing at the time of the above-mentioned record and playback from the same reference clock.
[Claim 5] It is the video camera according to claim 1 characterized by the above-mentioned timing generating means synchronizing timing of a packet of the 1 above-mentioned field unit with a power line period of the alternating current lighting lighting concerned in the case of photography under alternating current lighting lighting.
[Claim 6] a control method of a video camera characterized by being the control method of a video camera that time-axis elongation or compression of an image can be performed, for a picture signal from the above-mentioned image sensor carrying out reading appearance, and treating timing at the time of record of the picture signal concerned as a packet of 1 field unit, and fixed-izing a data rate in the packet concerned while performing record playback of a picture signal picturized with an image sensor.
[Claim 7] The above-mentioned packet is the control method of a video camera according to claim 6 characterized by being from a sensor gate pulse to the above-mentioned image sensor before the Rhine shift termination of the 1 field.
[Claim 8] A data rate fixed-ized within the above-mentioned packet is the control method of a video camera according to claim 6 characterized by corresponding to a data rate of 1X.
[Claim 9] Timing of the above-mentioned record playback is the control method of a video camera according to claim 6 characterized by generating from the same reference clock.
[Claim 10] A control method of a video camera according to claim 6 characterized by synchronizing timing of a packet of the 1 above-mentioned field unit with a power line period of the alternating current lighting lighting concerned in the case of photography under alternating current lighting lighting.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] It relates to the video camera which can perform time-axis elongation or compression of an image, and its control method while record playback of a picture signal is possible for this invention.
[0002]
[Description of the Prior Art] Conventionally, there is a time-axis transformation method in the commercial image and image work of art which consist of a dynamic image represented by slow motion as a way method for directing the texture of a photographic subject.
[0003] Conventionally, this time-axis conversion was performed by taking a photograph at the field rate at the time of projection, and a different rate with a film camera. That is, when rate ****** quicker than the field rate for example, at the time of projection is performed and it is made to perform projection at the usual field rate at the time of projection at the time of photography, a slow motion image will be acquired at the time of the projection concerned. In addition, such a slow motion image can be said to be the image which the time-axis elongated rather than the actual image time-axis.
[0004] However, by the method of the time-axis conversion by this film camera, unless the photoed film is developed, the effect of production cannot be checked and there is a defect that there is no sex instancy.
[0005]
[Problem(s) to be Solved by the Invention] On the other hand, if time-axis conversion is realizable in a video camera, for example, since the record medium in which the record playback which has a sex magnetic and electric instancy is possible can be used, the effect of production can be immediately checked after photography.
[0006] However, generally, in order that a video camera may follow the present broadcast format of NTSC (National Television SystemCommittee), PAL (Phase Alternation by Line), SECAM (sequential a memoire color television system), etc., etc., that by which the frame rate is being fixed to 30 or 25-frame per second is almost the case. the frame rate which serves as criteria as an exception — ready — although the video camera which realizes severalX also exists, in the point of the production of the texture of an image, expressional flexibility is scarce.
[0007] Here, in a video camera, if it is going to realize elongation and compression of the time-axis of the image of an image by changing the reference clock of a recording system, in order for (1) video signal band to change, it is necessary to change the property of a filter.
(2) It is necessary using a delay line to change the amount of delay of the circuit which is carrying out timing adjustment.
(3) A timing synchronous circuit with a reversion system becomes complicated. There was a said defect.
[0008] Then, this invention aims at offering the video camera which enables time-axis conversion simply and easily, and its control method, without also making the circuit for a timing synchronization of a recording system and a reversion system complicate, without being made in view of the actual condition mentioned above, and changing a filter shape, the amount of delay, etc.
[0009]
[Means for Solving the Problem] a video camera and its control method of this invention solve a technical problem mentioned above by a picture signal from an image sensor carrying out reading appearance, and treating timing at the time of record of the picture signal concerned as a packet of 1 field unit, and fixed-izing a data rate in the packet concerned.
[0010] According to this invention, although a data rate in a packet is fixed-ized to a data rate corresponding to 1X, modification of a rate, i.e., a field rate, for every packet to arbitration is enabled. For this reason, a field rate of arbitration can be realized, without adding modification to a digital disposal circuit.
[0011]
[Embodiment of the Invention] Hereafter, the gestalt of desirable operation of this invention is explained, referring to a drawing.
[0012] The whole video camera configuration of the gestalt of the 1 operation by which the video camera and its control method of this invention are applied to drawing 1 is shown.
[0013] In this drawing 1 , the CCD (Charge Coupled Devise) imager 1 changes into a picture signal images, such as a photographic subject in which image formation was carried out on the light-receiving side by the optical system which is not illustrated, by photo electric conversion. The picture signal generated by the photo electric conversion

in this CCD imager 1 is sent to the processor circuit 2. In this processor circuit 2, predetermined video signal processing is performed to a picture signal from the CCD imager 1. In addition, predetermined video signal processing in this processor circuit 2 is performed by the usual video camera, and since it is common knowledge, that explanation is omitted here. A carrier beam picture signal is sent and recorded on the record playback section 3 equipped with either or those combination, such as RAM (Random Access Memory), a hard disk, and a video tape, as a record medium in video signal processing in the processor circuit 2 concerned. In the gestalt of this operation, if drive timing of the above-mentioned CCD imager 1 and write-in timing of the picture signal in the record playback section 3 are made into the frame rate of arbitration 3X or less, they can do ** and the record timing generator 5 will manage them.

[0014] On the other hand, the criteria synchronizing signal supplied through the terminal 9 from the synchronizing signal generating circuit which is not illustrated is inputted into the playback timing generator 6. Synchronizing with the criteria synchronizing signal concerned, the playback timing managed with the playback timing generator 6 is reproduced by the 1X frame rate, and the picture signal currently recorded on the above-mentioned record playback section 3 is sent to the processor circuit 4. In this processor circuit 4, predetermined signal processing is performed to the signal supplied from the record playback section 3, and the acquired picture signal is outputted to the latter part from the video outlet terminal 8. In addition, predetermined video signal processing in this processor circuit 4 is performed by the usual video camera, and since it is common knowledge, that explanation is omitted here.

[0015] A system controller 7 performs the synchronousr control of the above-mentioned record timing generator 5 and the playback timing generator 6 while controlling each part.

[0016] As mentioned above, time-axis conversion of an image will be performed by making drive timing of the above-mentioned CCD imager 1, and write-in timing of the record playback section 3 into the frame rate of arbitration 3X or less, and making the time of the playback from the record playback section 3 into a 1X frame rate by one side. That is, if drive timing of the above-mentioned CCD imager 1 and write-in timing of the record playback section 3 are made into a 3X frame rate and the time of the playback from the record playback section 3 is made into a 1X frame rate for example, the image outputted to the latter part will turn into a slow motion image with which the time-axis was elongated 3 times from the video outlet terminal 8.

[0017] The timing chart of the various CCD driving signals sent to the CCD imager 1 at the time of applying the video camera of the gestalt of this operation which realizes the above-mentioned time-axis conversion to a system of 525 lines / 60 field per second like NTSC system from the above-mentioned record timing generator 5 is shown in drawing 2 . VD in drawing 2 shows the field packet to which CG mentions a perpendicular register transfer clock later, and, as for FP, V1, V2, V3, and V4 mention a sensor gate pulse for the vertical driving pulse of the CCD imager 1 later, EL shows effective Rhine, and drawing 2 (a) shows the timing chart of the even field (even number field) to drawing 2 (b) for the timing chart of the od field (odd number field).

[0018] Here, speed of a CCD drive is made into 3 usual times to CCD drive timing as shown in this drawing 2 . Speaking concretely, an adjustable frame rate's 3X or less being realizable by controlling the timing which starts two kinds of field packets FP of odd number even number (the od, even) by making timing from the sensor gate pulse CG of the CCD imager 1 to the Rhine shift termination of the 1 field into the field packet FP.

[0019] Namely, as shown in the table and drawing 4 of drawing 3 , the period which performs the level vertical drive of the CCD imager 1 constantly [usual] at 3X, and stands the sensor gate pulse CG By changing according to a desired field rate, photography by speed, such as 3X or less, for example, 1X, 1.5X, 2X, 2.5X, and 3X, and photography by speed, such as 1 moreX or less, for example, 0.5X etc., are attained. In addition, the conversion table of a field rate and a packet period is shown in drawing 3 . A packet period in case field rates are 30 fields / second (namely, 0.5X) For example, 3150 lines/frame A packet period in case field rates are 45 fields / second (namely, 0.75X) 2100 lines/frame A packet period in case field rates are 60 fields / second (namely, one X) 1575 lines/frame Becoming ..., in the following, a packet period in case 630 lines/frame and the field rate of a packet period in case field rates are the 150 fields / second (namely, 2.5X) are the 180 fields / second (namely, three X) becomes the same a frame in 525 lines /. Moreover, when field rates are the 180 fields / second (namely, three X), the sensor gate pulse CG at the time of 60 fields / second (one X) and the timing of a field packet period are shown in drawing 4 (a) at drawing 4 (b) at drawing 4 (c) at the time of 90 fields / second (namely, 1.5X).

[0020] As mentioned above, according to the gestalt of this operation, the time-axis of an image can be elongated or compressed by adopting the concept of the field packet FP and changing the period which stands the sensor gate pulse CG according to a desired field rate.

[0021] Moreover, according to the gestalt of this operation, within the field packet FP, even if a frame rate changes, since CCD level drive frequency is always fixed-ized, modification does not have necessity in the analog signal processing circuit which influences image quality, such as timing of an image frequency band or sample hold, therefore the stable image is acquired. About an analog signal processing circuit, it mentions later.

[0022] Furthermore, even if the writing and read-out timing to the record playback section 3 are made from the same reference clock and a field rate changes, since level timing is eternal, it can respond only by modification of the Rhine unit and a synchronous system is simple [timing] according to the gestalt of this operation.

[0023] Although the flicker in low frequency will be conspicuous under alternating current lighting lighting, such as a fluorescent lamp, in addition to this when performing speed photography of source-power-supply frequency (Japan 60Hz or 50Hz) of 1 time or about 2 times, in the video camera of the gestalt of this operation, a flicker can be lost by synchronizing the field timing of a recording system with source-power-supply frequency.

[0024] The example of 1 configuration of an analog signal processing circuit is shown in drawing 5 .

[0025] In this drawing 5 , the picture signal outputted from the CCD imager 11 is sent to a sample hold circuit 12. In the sample hold circuit 12 concerned, an analog picture signal is sampled and held and the picture signal sampled and held is sent to the shading compensating network 13. These CCD imager 11 and a sample hold circuit 12 operate based on the timing signal from the CCD drive timing generator 17.

[0026] The shading compensating network 13 performs shading compensation (amendment) processing which superimposes the approximation saw tooth wave which synchronized with the horizontal and vertical scan supplied from H and V approximation saw-tooth-wave radionuclide generator 18 on a picture signal from a sample hold circuit 12.

[0027] The picture signal outputted from the shading compensating network 13 is changed into digital image data by the analog / digital (A/D) converter 15, after a higher-harmonic noise component is removed by the low pass filter (LPF). This image data is sent to a latter configuration from an output terminal 16.

[0028]

[Effect of the Invention] in this invention, time-axis conversion is easily [simply and] possible, without also making the circuit for a timing synchronization of a recording system and a reversion system complicate, without adding modification to the digital disposal circuit of a filter shape or the amount of delay by the picture signal from an image sensor carrying out reading appearance, and treating the timing at the time of record of the picture signal concerned as a packet of 1 field unit, and fixed-izing the data rate in the packet concerned.

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TECHNICAL FIELD

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PRIOR ART

[Description of the Prior Art] Conventionally, there is a time-axis transformation method in the commercial image and image work of art which consist of a dynamic image represented by slow motion as a way method for directing the texture of a photographic subject.
[0003] Conventionally, this time-axis conversion was performed by taking a photograph at the field rate at the time of projection, and a different rate with a film camera. That is, when rate ****** quicker than the field rate for example, at the time of projection is performed and it is made to perform projection at the usual field rate at the time of projection at the time of photography, a slow motion image will be acquired at the time of the projection concerned. In addition, such a slow motion image can be said to be the image which the time-axis elongated rather than the actual image time-axis.
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TECHNICAL PROBLEM

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MEANS

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[Embodiment of the Invention] Hereafter, the gestalt of desirable operation of this invention is explained, referring to a drawing.

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[0015] A system controller 7 performs the synchronousr control of the above-mentioned record timing generator 5 and the playback timing generator 6 while controlling each part.

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[0017] The timing chart of the various CCD driving signals sent to the CCD imager 1 at the time of applying the video camera of the gestalt of this operation which realizes the above-mentioned time-axis conversion to a system of 525 lines / 60 field per second like NTSC system from the above-mentioned record timing generator 5 is shown in drawing 2 . VD in drawing 2 shows the field packet to which CG mentions a perpendicular register transfer clock later, and, as for FP, V1, V2, V3, and V4 mention a sensor gate pulse for the vertical driving pulse of the CCD imager 1 later, EL shows effective Rhine, and drawing 2 (a) shows the timing chart of the even field (even number field) to drawing 2 (b) for the timing chart of the od field (odd number field).

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[0024] The example of 1 configuration of an analog signal processing circuit is shown in drawing 5 .

[0025] In this drawing 5 , the picture signal outputted from the CCD imager 11 is sent to a sample hold circuit 12. In the sample hold circuit 12 concerned, an analog picture signal is sampled and held and the picture signal sampled and held is sent to the shading compensating network 13. These CCD imager 11 and a sample hold circuit 12 operate based on the timing signal from the CCD drive timing generator 17.

[0026] The shading compensating network 13 performs shading compensation (amendment) processing which superimposes the approximation saw tooth wave which synchronized with the horizontal and vertical scan supplied from H and V approximation saw-tooth-wave radionuclide generator 18 on a picture signal from a sample hold circuit 12.

[0027] The picture signal outputted from the shading compensating network 13 is changed into digital image data by the analog / digital (A/D) converter 15, after a higher-harmonic noise component is removed by the low pass filter (LPF). This image data is sent to a latter configuration from an output terminal 16.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block circuit diagram showing the outline configuration of the video camera of the gestalt of this invention operation.
[Drawing 2] It is the timing chart of the CCD driving signal at the time of applying the video camera of the gestalt of this operation to the system of 525 lines / 60 field per second.
[Drawing 3] It is drawing showing the conversion table of a field rate and a packet period.
[Drawing 4] It is the timing chart which shows the sensor gate pulse at the time of 3X, 1.5X, and 1X photography, and the timing of a field packet period.
[Drawing 5] It is the block circuit diagram showing the example of 1 configuration of an analog signal processing circuit.
[Description of Notations]
1 CCD Imager 2 Four Processor Circuit 3 Record Playback Section 5 Record Timing Generator 6 Playback Timing Generator 7 System Controller

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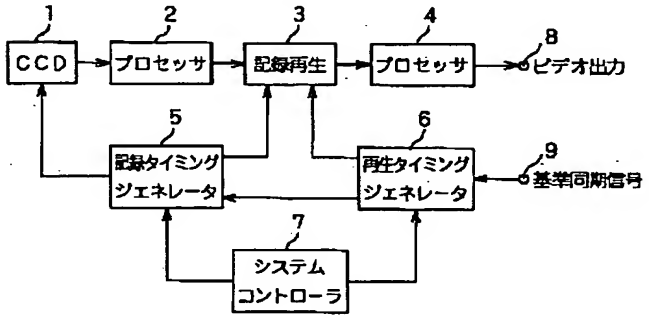
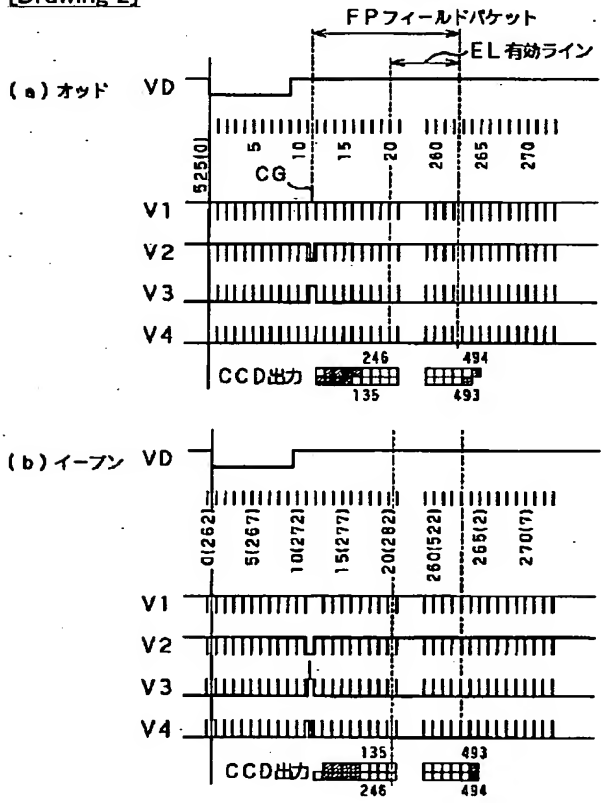
DRAWINGS

[Drawing 1]



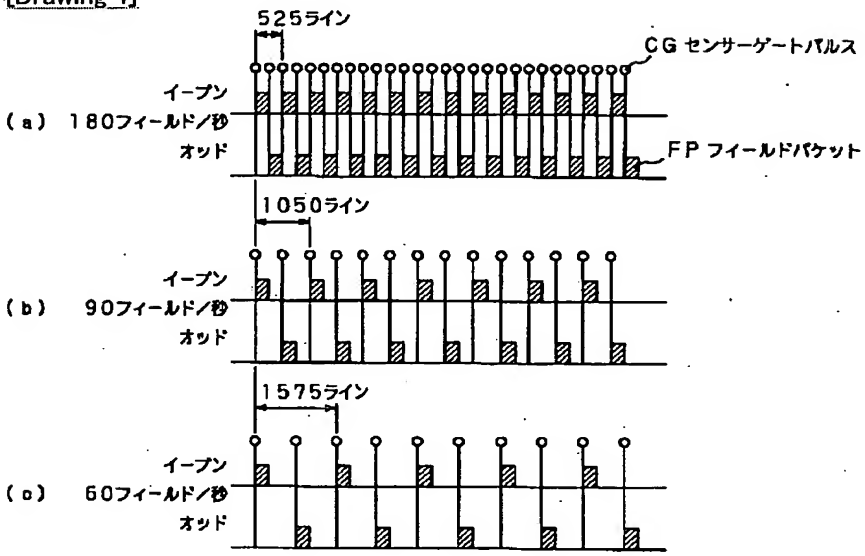
[Drawing 2]



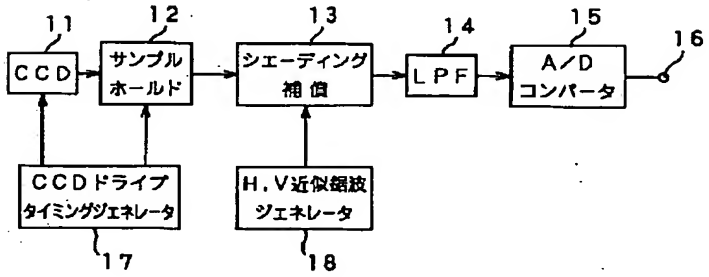
[Drawing 3]

フィールド/秒	ライン/フレーム
30	3150
45	2100
60	1575
75	1260
90	1050
100	945
125	756
150	630
180	525

[Drawing 4]



[Drawing 5]



[Translation done.]

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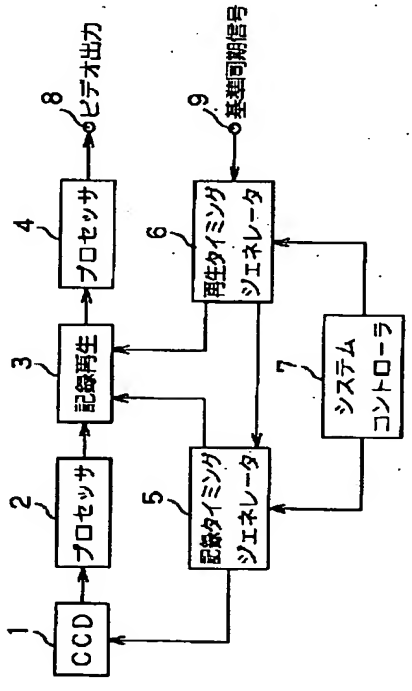
(54)【発明の名称】　ビデオカメラ及びその制御方法

(57)【要約】

【課題】　フィルタ特性やディレイ量等を変えることなく、また記録系と再生系とのタイミング同期用回路も複雑化させずに、簡単且つ容易に時間軸変換を実現する。

【解決手段】　ＣＣＤイメージャ１にて撮像した画像信号を記録再生部３にて記録再生すると共に、映像の時間軸伸張又は圧縮を行い得るビデオカメラであり、ＣＣＤイメージャ１の駆動信号及び記録タイミング信号を発生する記録タイミングジェネレータ５を有し、この記録タイミングジェネレータ５は、ＣＣＤイメージャ１からの画像信号の読み出し及び該画像信号の記録時のタイミングを、１フィールド単位のパケットとして扱うと共に、当該パケット内のデータレートを１倍速のレートに一定化させる。



【特許請求の範囲】
【請求項１】　撮像素子にて撮像した画像信号の記録再生を行うと共に、映像の時間軸伸張又は圧縮を行い得るビデオカメラであって、
上記撮像素子の駆動信号及び記録時のタイミング信号を少なくとも発生するタイミング発生手段を有し、
当該タイミング発生手段は、上記撮像素子からの画像信号の読み出し及び当該画像信号の記録時のタイミングを、１フィールド単位のパケットとして扱うと共に、当該パケット内のデータレートを一定化させることを特徴とするビデオカメラ。
【請求項２】　上記タイミング発生手段は、上記撮像素子へのセンサゲートパルスから１フィールドのラインシフト終了までの間を上記パケットとすることを特徴とする請求項１記載のビデオカメラ。
【請求項３】　上記タイミング発生手段は、上記パケット内のデータレートを１倍速に一定化させることを特徴とする請求項１記載のビデオカメラ。
【請求項４】　上記タイミング発生手段は、記録した画像信号の再生時のタイミング信号をも発生し、上記記録時と再生時のタイミングを同一の基準クロックから生成することを特徴とする請求項１記載のビデオカメラ。
【請求項５】　交流点灯照明下での撮影の際に、上記タイミング発生手段は上記１フィールド単位のパケットのタイミングを当該交流点灯照明の電源周波数と同期させることを特徴とする請求項１記載のビデオカメラ。
【請求項６】　撮像素子にて撮像した画像信号の記録再生を行うと共に、映像の時間軸伸張又は圧縮を行い得るビデオカメラの制御方法であって、
上記撮像素子からの画像信号の読み出し及び当該画像信号の記録時のタイミングを、１フィールド単位のパケットとして扱い、当該パケット内のデータレートを一定化することを特徴とするビデオカメラの制御方法。
【請求項７】　上記パケットは、上記撮像素子へのセンサゲートパルスから１フィールドのラインシフト終了までの間であることを特徴とする請求項６記載のビデオカメラの制御方法。
【請求項８】　上記パケット内で一定化するデータレートは１倍速のデータレートに対応することを特徴とする請求項６記載のビデオカメラの制御方法。
【請求項９】　上記記録再生のタイミングは同一の基準クロックから生成することを特徴とする請求項６記載のビデオカメラの制御方法。
【請求項１０】　交流点灯照明下での撮影の際には、上記１フィールド単位のパケットのタイミングを、当該交流点灯照明の電源周波数と同期させることを特徴とする請求項６記載のビデオカメラの制御方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、画像信号の記録再生が可能であると共に映像の時間軸伸張又は圧縮を行い得るビデオカメラ及びその制御方法に関する。
【０００２】
【従来の技術】従来より、動画像からなるコマーシャル映像や映像芸術作品における、被写体の質感を演出するための一手法として、スローモーションに代表される時間軸変換法がある。
【０００３】従来、この時間軸変換は、フィルムカメラによって映写時のフィールドレートと異なるレートで撮影することにより行われていた。すなわち、撮影時に例えば映写時のフィールドレートよりも速いレートて撮影を行い、映写時には通常のフィールドレートでの映写を行うようにすると、当該映写時にはスローモーション映像が得られることになる。なお、このようなスローモーション映像は、現実の映像時間軸よりも時間軸が伸張した映像と言える。
【０００４】しかし、このフィルムカメラによる時間軸変換の方式では、撮影したフィルムを現像しない限り、演出の効果が確認できなく、即時性が無いという欠点がある。
【０００５】
【発明が解決しようとする課題】これに対して、例えばビデオカメラにおいて時間軸変換を実現できれば、磁気的、電気的な即時性のある記録再生が可能な記録媒体を用いることができるので、演出の効果を、撮影後直ちに確認できることになる。
【０００６】しかし、一般的に、ビデオカメラは、ＮＴＳＣ（National Television SystemCommittee）やＰＡＬ（Phase Alternation by Line）、ＳＥＣＡＭ（sequential a memoire color television system）等の現行放送フォーマットに従うため、フレームレートが３０或いは２５フレーム毎秒に固定されているものが殆どである。例外として、基準となるフレームレートの整数倍速を実現するビデオカメラも存在するが、映像の質感の演出という点においては表現の自由度が乏しい。
【０００７】ここで、ビデオカメラにおいて、映像の映像の時間軸の伸張や圧縮を例えば記録系の基準クロックを変えることによって実現しようとすると、
（１）映像信号帯域が変わるため、フィルタの特性を変える必要がある。
（２）ディレイラインを用いて、タイミング調整をしている回路のディレイ量を変える必要がある。
（３）再生系とのタイミング同期回路が複雑になる。といった欠点があった。
【０００８】そこで、本発明は、上述した実情に鑑みてなされたものであり、フィルタ特性やディレイ量等を変えることなく、また記録系と再生系とのタイミング同期用回路も複雑化させずに、簡単且つ容易に時間軸変換を可能とするビデオカメラ及びその制御方法を提供することを目的とする。

【０００９】
【課題を解決するための手段】本発明のビデオカメラ及びその制御方法は、撮像素子からの画像信号の読み出し及び当該画像信号の記録時のタイミングを、１フィールド単位のパケットとして扱い、当該パケット内のデータレートを一定化することにより、上述した課題を解決する。
【００１０】本発明によれば、パケット内のデータレートは例えば１倍速に対応するデータレートに一定化するが、パケット毎のレートすなわちフィールドレートを任意に変更可能にしている。このため、任意のフィールドレートを信号処理回路に変更を加えることなく実現可能となっている。
【００１１】
【発明の実施の形態】以下、本発明の好ましい実施の形態について、図面を参照しながら説明する。
【００１２】図１に、本発明のビデオカメラ及びその制御方法が適用される一実施の形態のビデオカメラの全体構成を示す。
【００１３】この図１において、ＣＣＤ（Charge Coupled Devise）イメージャ１は、図示しない光学系によって受光面上に結像された被写体等の像を光電変換により画像信号に変換する。このＣＣＤイメージャ１での光電変換により生成された画像信号は、プロセッサ回路２に送られる。このプロセッサ回路２では、ＣＣＤイメージャ１からの画像信号に所定の映像信号処理を施す。なお、このプロセッサ回路２における所定の映像信号処理は、通常のビデオカメラにて行われるものであり、周知であるためここではその説明を省略する。当該プロセッサ回路２にて映像信号処理を受けた画像信号は、記録媒体として例えばＲＡＭ（Random Access Memory）、ハードディスク、ビデオテープ等の何れか若しくはそれらの組み合わせを備える記録再生部３に送られて記録される。本実施の形態において、上記ＣＣＤイメージャ１の駆動タイミングと記録再生部３における画像信号の書き込みタイミングは、３倍速以下の任意のフレームレートにするとこができ、記録タイミングジェネレータ５が管理する。
【００１４】一方で、再生タイミングジェネレータ６には、図示しない同期信号発生回路から端子９を介して供給された基準同期信号が入力される。上記記録再生部３に記録されている画像信号は、当該基準同期信号に同期して、再生タイミングジェネレータ６で管理された再生タイミングにより１倍速のフレームレートで再生され、プロセッサ回路４に送られる。このプロセッサ回路４では、記録再生部３から供給された信号に所定の信号処理を施し、得られた画像信号がビデオ出力端子８から後段に出力される。なお、このプロセッサ回路４における所定の映像信号処理は、通常のビデオカメラにて行われるものであり、周知であるためここではその説明を省略する。
【００１５】システムコントローラ７は、各部の制御を行うと共に、上記記録タイミングジェネレータ５と再生タイミングジェネレータ６の同期制御を行う。
【００１６】上述のように、上記ＣＣＤイメージャ１の駆動タイミングと記録再生部３の書き込みタイミングを３倍速以下の任意のフレームレートにし、一方で、記録再生部３からの再生時を１倍速のフレームレートにすることで、映像の時間軸変換が行われることになる。すなわち例えば、上記ＣＣＤイメージャ１の駆動タイミングと記録再生部３の書き込みタイミングを３倍速のフレームレートにし、記録再生部３からの再生時を１倍速のフレームレートにすると、ビデオ出力端子８から後段に出力される画像は３倍に時間軸が伸張されたスローモーション映像となる。
【００１７】図２には、例えばＮＴＳＣ方式のような５２５ライン／６０フィールド毎秒のシステムに、上記時間軸変換を実現する本実施の形態のビデオカメラを適用した場合の、上記記録タイミングジェネレータ５からＣＣＤイメージャ１に送られる各種ＣＣＤ駆動信号のタイミングチャートを示す。図２中のＶＤはＣＣＤイメージャ１の垂直駆動パルスを、Ｖ１，Ｖ２，Ｖ３，Ｖ４は垂直レジスタ転送クロックを、ＣＧはセンサゲートパルスを、ＦＰは後述するフィールドパケットを、ＥＬは有効ラインを示し、図２（ａ）はオッドフィールド（奇数フィールド）のタイミングチャートを、図２（ｂ）にはイーブンフィールド（偶数フィールド）のタイミングチャートを示している。
【００１８】ここで、この図２に示すようなＣＣＤ駆動タイミングに対して、ＣＣＤ駆動のスピードを例えば通常の３倍とする。具体的に言うと、ＣＣＤイメージャ１のセンサゲートパルスＣＧから、１フィールドのラインシフト終了までのタイミングをフィールドパケットＦＰとして、奇数偶数（オッド、イーブン）の２種類のフィールドパケットＦＰを開始するタイミングを制御することで、３倍速以下の可変フレームレートを実現することができる。
【００１９】すなわち、ＣＣＤイメージャ１の水平垂直駆動を、例えば通常の３倍速でコンスタントに行い、センサゲートパルスＣＧを立てる周期を、図３の表及び図４に示すように、所望のフィールドレートに応じて変えることにより、３倍速以下、例えば１倍速、１．５倍速、２倍速、２．５倍速、３倍速等のスピードでの撮影や、更に１倍速以下、例えば０．５倍速等のスピードでの撮影が可能となる。なお、図３には、フィールドレートとパケット周期の対応表を示しており、例えばフィールドレートが３０フィールド／秒（すなわち０．５倍速）のときのパケット周期は３１５０ライン／フレーム、フィールドレートが４５フィールド／秒（すなわち０．７５倍速）のときのパケット周期は２１００ライン

／フレーム、フィールドレートが６０フィールド／秒（すなわち１倍速）のときのパケット周期は１５７５ライン／フレーム、・・・となり、以下同様に、フィールドレートが１５０フィールド／秒（すなわち２．５倍速）のときのパケット周期は６３０ライン／フレーム、フィールドレートが１８０フィールド／秒（すなわち３倍速）のときのパケット周期は５２５ライン／フレームとなる。また、図４（ａ）にはフィールドレートが１８０フィールド／秒（すなわち３倍速）のとき、図４（ｂ）には９０フィールド／秒（すなわち１．５倍速）のとき、図４（ｃ）には６０フィールド／秒（１倍速）のときのセンサゲートパルスＣＧとフィールドパケット周期のタイミングを示している。

【００２０】上述のように、本実施の形態によれば、フィールドパケットＦＰという概念を採用し、センサゲートパルスＣＧを立てる周期を所望のフィールドレートに応じて変えることにより、映像の時間軸を伸張或いは圧縮することができる。

【００２１】また、本実施の形態によれば、フレームレートが変化しても、フィールドパケットＦＰ内ではＣＣＤ水平駆動周波数を常に一定化しているため、映像周波数帯域やサンプルホールドのタイミング等、画質に影響するアナログ信号処理回路に変更は必要無く、したがって安定した映像が得られる。アナログ信号処理回路については後述する。

【００２２】さらに、本実施の形態によれば、記録再生部３に対する書き込み及び読み出しタイミングが同一の基準クロックから作られ、フィールドレートが変わっても水平タイミングは不変なので、ライン単位の変更のみで対応でき、同期系が単純である。

【００２３】その他、例えば蛍光灯等の交流点灯照明下で、商用電源周波数（日本国では６０Ｈｚ或いは５０Ｈｚ）の１倍或いは２倍程度のスピード撮影を行う場合には、低い周波数でのフリッカが目立つことになるが、本実施の形態のビデオカメラにおいては、記録系のフィールドタイミングを商用電源周波数に同期させることにより、フリッカを無くすことができる。

【００２４】図５には、アナログ信号処理回路の一構成例を示す。

【００２５】この図５において、ＣＣＤイメージャ１１から出力された画像信号は、サンプルホールド回路１２に送られる。当該サンプルホールド回路１２では、アナログ画像信号を標本化して保持し、その標本化して保持した画像信号をシェーディング補償回路１３に送る。これらＣＣＤイメージャ１１及びサンプルホールド回路１２は、ＣＣＤドライブタイミングジェネレータ１７からのタイミング信号に基づいて動作する。

【００２６】シェーディング補償回路１３は、Ｈ，Ｖ近似鋸波ジェネレータ１８から供給された水平及び垂直の走査に同期した近似鋸波を、サンプルホールド回路１２からの画像信号に重畳するシェーディング補償（補正）処理を行う。

【００２７】シェーディング補償回路１３から出力された画像信号は、ローパスフィルタ（ＬＰＦ）にて高調波ノイズ成分が除去された後、アナログ／ディジタル（Ａ／Ｄ）コンバータ１５にてディジタル画像データに変換される。この画像データは出力端子１６から後段の構成に送られる。

【００２８】

【発明の効果】本発明においては、撮像素子からの画像信号の読み出し及び当該画像信号の記録時のタイミングを、１フィールド単位のパケットとして扱い、当該パケット内のデータレートを一定化することにより、フィルタ特性やディレイ量の信号処理回路に変更を加えることなく、また記録系と再生系のタイミング同期用回路も複雑化させずに、簡単且つ容易に時間軸変換が可能である。

【図面の簡単な説明】

【図１】本発明実施の形態のビデオカメラの概略構成を示すブロック回路図である。

【図２】５２５ライン／６０フィールド毎秒のシステムに、本実施の形態のビデオカメラを適用した場合のＣＣＤ駆動信号のタイミングチャートである。

【図３】フィールドレートとパケット周期の対応表を示す図である。

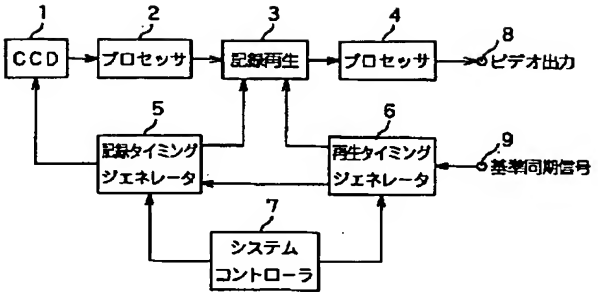
【図４】３倍速、１．５倍速、１倍速撮影のときのセンサゲートパルスとフィールドパケット周期のタイミングを示すタイミングチャートである。

【図５】アナログ信号処理回路の一構成例を示すブロック回路図である。

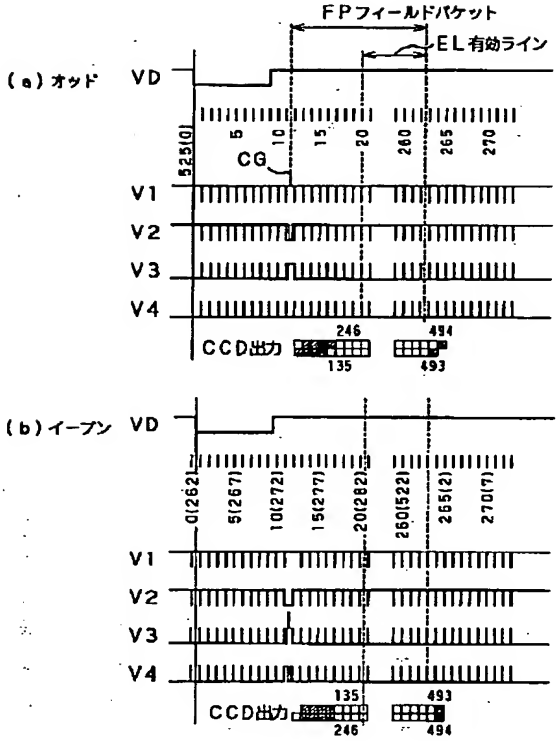
【符号の説明】

１　ＣＣＤイメージャ、　２，４　プロセッサ回路、
３　記録再生部、　５記録タイミングジェネレータ、
６　再生タイミングジェネレータ、　７　システムコントローラ

【図１】



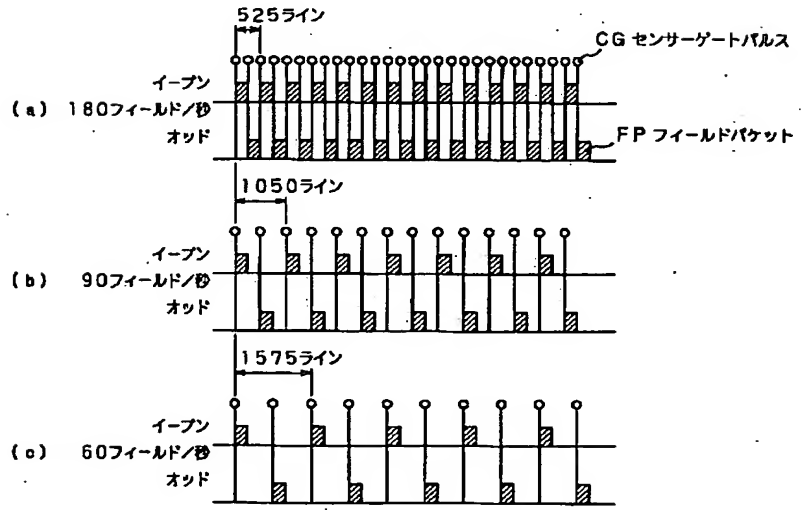
【図２】



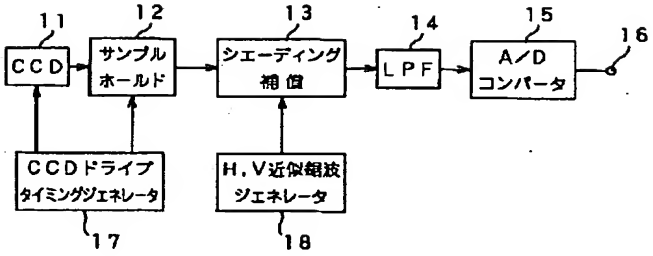
【図３】

フィールド/秒	ライン/フレーム
30	3150
45	2100
60	1575
75	1260
90	1050
100	945
125	756
150	630
180	525

【図４】



【図５】


11
CCD
12
サンプル
ホールド
13
シェーディング
補 償
14
LPF
15
A／D
コンバータ
16
CCDドライブ
タイミングジェネレータ
17
H，V近似矩波
ジェネレータ
18